A Generic Multi-Modulus Divider Architecture for Fractional-*N* Frequency Synthesisers

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***Abstract*—This paper describes the design of a new technique and architecture of multi-modulus divider for Sigma-Delta fractional-*N* PLL frequency synthesisers. The proposed architecture uses a memory-controlled technique that can achieve a wider range of prescaler modulus values, more flexible operation, and lower power dissipation. It has been implemented in an FPGA in conjunction the store-sequence architecture and a range of Sigma-Delta modulators. Both simulated and measured results are shown to demonstrate that a substantial improvement in performance is possible.**

I. INTRODUCTION

Dual modulus prescalers are used in frequency synthesisers as a cost effective solution with transparent worldwide usage. They have many merits: simple architecture, high operating frequency, low cost and good power efficiency. However, as wireless communication systems develop, the need for fine channel resolution, fast tuning and high spectral purity has led to the adoption of multi-level Σ-Δ modulators that, of course, require multi-modulus dividers. Therefore, multi-modulus dividers have been playing an increasingly significant role in Σ-Δ fractional-*N* frequency synthesis. Fig. 1 shows an arrangement of a Σ-Δ fractional-*N* PLL frequency synthesiser suitable for the GSM system, which indicates the need for a Σ-Δ modulator and a multi-modulus divider to achieve fractional-*N* division. In a synthesiser context, this provides a fractional mean division ratio with low close-in phase noise at the expense of increased phase noise further from the carrier where it may be readily suppressed by the action of the PLL filter [1]. High-frequency programmable dividers are invariably based on one or two established techniques involving either a single multi-modulus prescaler and associated counters and control logic or cascaded ÷2/3 prescalers with associated control logic [2].

This paper presents a new technique of multi-modulus prescaler that can generate a wider range of modulus values which will achieve better noise shaping in fractional-*N* frequency synthesisers. Section 2 describes the proposed architecture and its comparison with conventional programmable dividers. Section 3 discusses the FPGA implementation and results in which a Σ-Δ fractional-*N* PLL frequency synthesiser based on the proposed technique is implemented and its performance is clearly demonstrated. The paper ends with a clear conclusion of the new multi-modulus divider and the future development of the memory controlled technique.

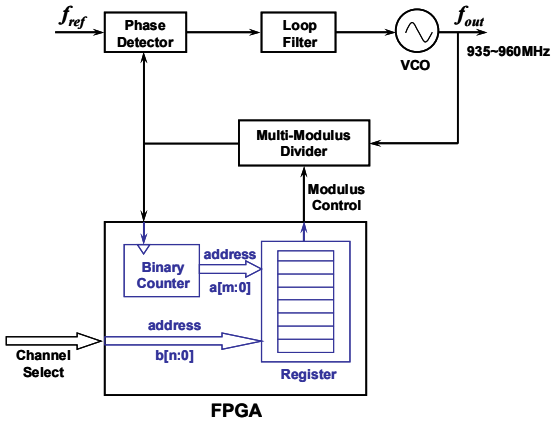

Figure 1. Fractional-N PLL frequency synthesiser.

II. PROPOSED TECHNIQUE AND ARCHITECTURE

A. *Ripple fashion Multi-Modulus prescaler*

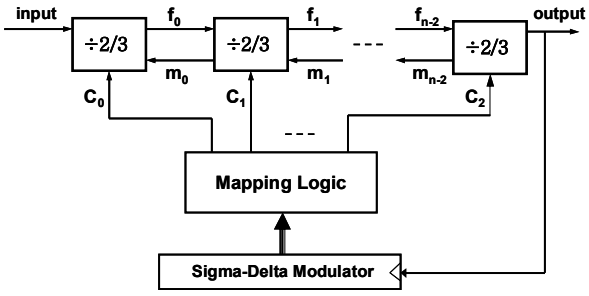

Figure 2. Conventional ripple flash multi-modulus divider.

A common ripple fashion architecture [3] [4] is shown in Fig. 2; the prescaler structure is based on the cascade of *n* 2/3 or *P*/*P*+1dual modulus blocks. Each 2/3 cell divides its input by 2 or 3 depending on its control signal c_n and feedback signal m_n. The feedback signal m_n is to prevent the cell from continuously dividing by 3, which leads to the lack of reusability of the building blocks. A cascade of *n* blocks can produce division ratios over the range 2^n to 2^{n+1}-1. The range of available modulus values is thus:

$$N_{RF} = 2^{n+1} - 2^n \quad (1)$$

If n equals 6, the divider has a 64-modulus with division ratios from 64 to 127.

B. Memory Controlled Technique

Fig. 3 shows the basic arrangement of the proposed divider technique. The 2/3 block can be replaced by any *P/P+1* block to achieve a variety of division ratios.

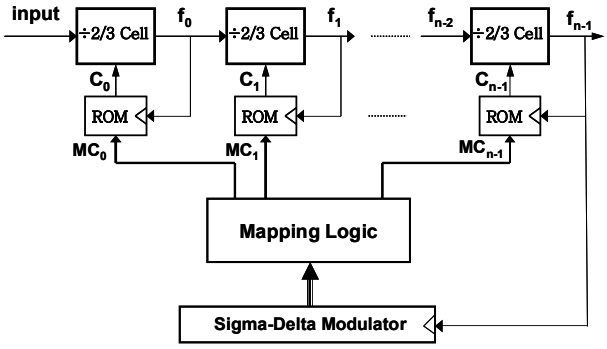

Figure 3. Memory-controlled multi-modulus divider

The output of the Σ-Δ modulator loads a word into an N-stage shift register. Each shift register is clocked by the prescaler output and determines its division ratio respectively. Cascading n 2/3 dual-modulus blocks can produce division ratio of 2^n to 3^n. The range of modulus values is now:

$$N_{MC} = 3^n - 2^n + 1 \quad (2)$$

The division ratio of this architecture is:

$$D = 2^n + M_0 \cdot 2^{n-1} + M_1 \cdot 2^{n-2} + \cdots + M_{n-1} \quad (3)$$

where:

$$0 \le M_p \le 3^{n-p} \quad (0 \le p \le n-1)$$

In which M_{n-1}, M_{n-2}, ... M_0 are divide-by-3 bits number of C_{n-1}, C_{n-2}, ... C_0 in a period of f_{n-1} respectively. Although its modulus range is much greater than that of the ripple fashion prescaler, ROMs must be introduced to control the division ratio of every block working under different frequencies. The total number of bits in the ROM is:

$$N_{bits} = \frac{3^n - 1}{2} \quad (4)$$

In this topology, 6 cascaded 2/3 cells result in a 666-modulus with division ratios from 64 to 729, which is 10.4 times of ripple fashion divider. At least a 364-bit ROM must be used to achieve the division control function. All division ratios in this range can be programmed with a unit increment. As mentioned before, the 2/3 block can be replaced by any *P/P+1* block, but all blocks should be the same to achieve unit increments. If an increment other than one is desired, the optimal architecture is to place a fixed ratio divide-by-N stage in front of the multi-modulus cells.

Compared with ripple fashion dividers, the proposed architecture has better reusability and programmability. By eliminating high frequency feedback signals and adding a high frequency memory control element, a main advantage of the memory controlled divider is that it efficiently uses every component and modulus repetition can be avoided by defining appropriate control signals derived from the proper Σ-Δ modulator output.

A simple lookup table can be used to derive the required values for the shift register control word needed to achieve a given division ratio. In terms of an FPGA or PLD implementation, all elements in the design apart from the prescaler are contained within the FPGA/PLD and so the technique presents a very convenient and efficient means of implementing a programmable high-frequency divider. Furthermore, other synthesiser operations, such as delta–sigma modulation for noise shaping, can be performed by the same FPGA or PLD, thus allowing integration of these functions in one device.

C. An memory-controlled 18-modulus divider

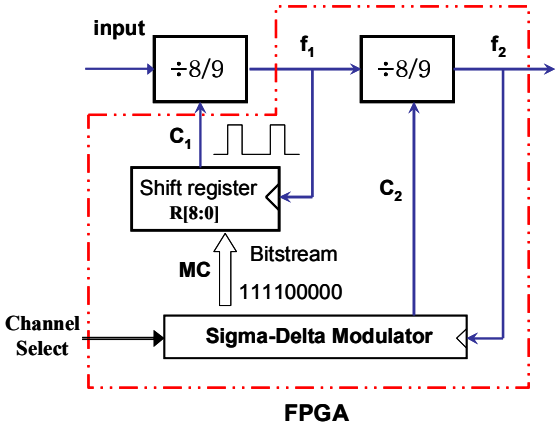

Figure 4. Memory controlled 18-modulus divider.

Let us now apply the generic memory-controlled technique to a GSM-900 transceiver design. Since synthesisers can have large power consumption and often occupy considerable area, it is very important to limit the number of components required by the radio architecture. Thus, for GSM-900 base stations, the required output frequency of the synthesiser is F_{VCO} = 935+0.2k MHz, where k=0,1,2…125. If a 12.8 MHz reference source is used, the division ratio needs to be:

$$D = \frac{F_{VCO}}{12.8} = 73.046875 + 0.015625k \quad (5)$$

i.e. D = 73.04625 ~ 75.

Assuming that a 3rd-order sigma-delta noise shaper with 3-bit output is used to remove the fractional spurs, the instantaneous division ratio could vary from -3 to 4 around the fractional mean division ratio. Thus, the division range is given by D = 70~77.

Fig. 4 shows an 18-modulus memory controlled divider that is designed to satisfy this requirement. The high-frequency VCO output signal is divided by two cascaded 8/9 prescalers. The output signal f_2 is around 12.8 MHz. It is compared with the reference frequency at the phase/frequency detector, which generates the phase difference signal [5]. Meanwhile, the Σ-Δ modulator is also controlled by f_2. At the rising edge of every f_2 cycles, the Σ-Δ modulator begins calculating one period and generates two modulus control bit streams: *MC* (9-bit) and

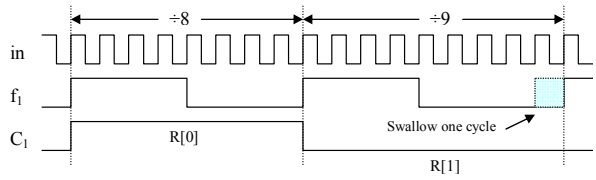

Figure 5. Modulus control function of the 8/9 block.

C_2 (1-bit). C_2 is directly employed to control the division ratio of the second 8/9 divider. When C_2 is logic-0, f_1 is divided by 9, which means this block swallows an extra single f_1 cycle in a complete division cycle, increasing the period of the output signal of this block by one period of f_1; when C_2 is logic-1 (high voltage), the output frequency f_2 is 8 times f_1. At the same time, a 9-bit word is loaded into a 9-stage shift register which is clocked by the 8/9 prescaler output and determines its division ratio. The total division ratio of this arrangement thus depends on the number, n, of logic-one bits that are presented to the shift register and is adjustable over the range 64 to 81. A time diagram of the 8/9 modulus control function is shown in Fig. 5. Each bit stored in the memory corresponds to a stable position signal result of f_1, meaning *R[3]* always only controls the fourth signal result of f_1 after each rising edge of f_2. This will reduce the complexity of the system. Its division ratio can be easily derived from (3):

$$D = 8 \times \left(\overline{C}_2 + 8\right) + M_{C_1} \quad \left(0 \le M_{C_1} \le 8\right) \qquad (6)$$

Suppose C_2 is low voltage and the bit stream of *MC* is 111 111 000, then M_{C1} is 3 and the first block will swallow 3 time cycles and the second will swallow 1. The division ratio of the complete cycle will be 75.

The 8/9 divider can be implemented using four D Latches and three logic gates as shown in Fig. 5(a). The components used and area occupation are similar to those of a divide by 2/3 block in a conventional programmable divider which is shown in Fig. 5(b). Hence the memory controlled divider will provide an approximate 50% saving on components and area even though some registers are needed. As discussed earlier, two cascaded 8/9 dividers can be merged into an 18 modulus divider, whose (integer) division ratio varies continuously between 64 and 81. This arrangement can synthesise all required frequencies in GSM or DCS system if connected to a Σ-Δ modulator with a 3 or more bits quantizer. If four dual modulus blocks are employed, the modulus can be extended to 180, which will satisfy a wide variety of wireless applications.

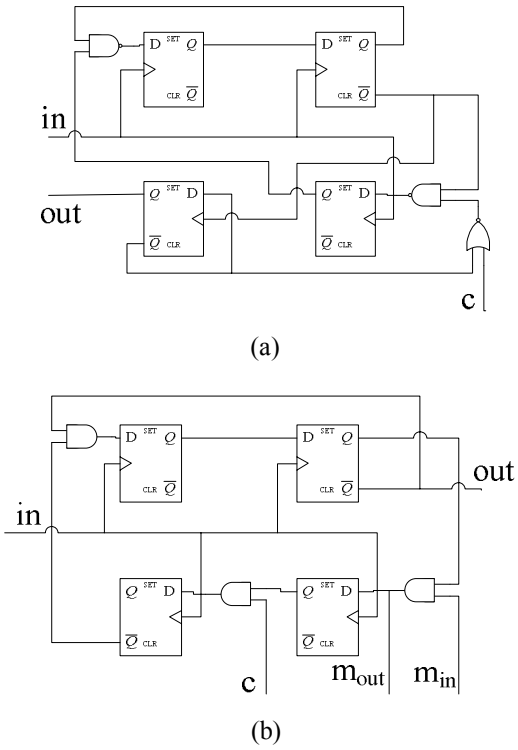

Figure 6. (a). Logical architecture of an 8/9 prescaler in memory controlled divider. (b). Logical architecture of a 2/3 prescaler in ripple fashion divider.

The technique may be combined with the 'stored-sequence' synthesiser approach [6] in which pre-generated modulator bitstreams are clocked out from memory in order to allow very fast loop operation and low phase noise. This presents a convenient, streamlined, architecture allowing a single block of memory to determine both noise shaping and prescaler modulus control and adds further to the elegance of the technique in an FPGA or PLD implementation [7].

III. Implementation and Results

The divider and Σ-Δ modulator design (dot line area in Fig. 3) are implemented on a Xilinx FPGA XC2V1500 having a maximum clock speed of 500 MHz in theory, allowing operation with a external 8/9 prescaler to a frequency of 3 GHz. The ISE simulation result of the 18-modulus divider is shown in Fig. 7. The 9-bit memory and the prescaler works under f_1, around 120 MHz, and all other parts work under f_2, around 12.8 MHz. Limited by the maximum frequency (about 450 MHz) of the FPGA testing board, the first 8/9 block cannot be implemented by FPGA. An additional 8/9 prescaler is employed to divider the VCO output frequency from 960 MHz to about 120

MHz. The third order single stage and MASH modulators [8] with 8-level outputs were also implemented in the same FPGA to control the divider.

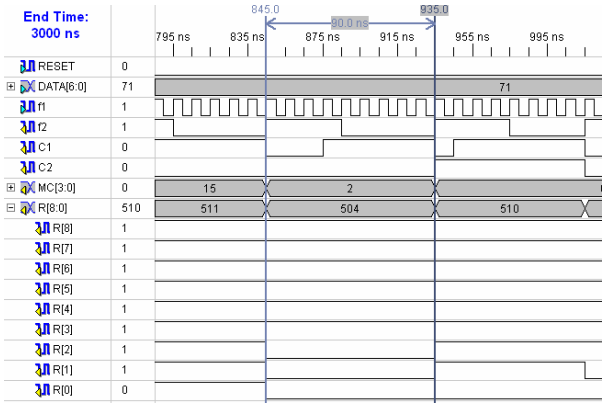

Figure 7. Behavioural simulation of an 18-modulus divider.

A prototype of fractional-N frequency synthesiser for the GSM-900 system has been successfully developed. This synthesiser solution is based on FPGA conjunction with external Phase/Frequency Detector, loop filter and VCO. Fig. 8 shows the open loop result of the prototype, in which the input is a stable 935 MHz oscillator. A third order single stage feedforward Σ-Δ modulator with a 3-bit (8-level) quantizer is used to suppress the close-in noise. The division ratio is $73+1/2+1/2^2+1/2^3+1/2^5+1/2^7+1/2^8+1/2^9$ =73.46. Fig. 9 shows the closed-loop output spectrum of the frequency synthesiser with the same division ratio. The structure and performance of the synthesiser is shown in Table 1. The phase noise of the carrier signal is dominated by reference noise at present, and it is hoped to obtain better performance by employing a reference source with lower phase noise.

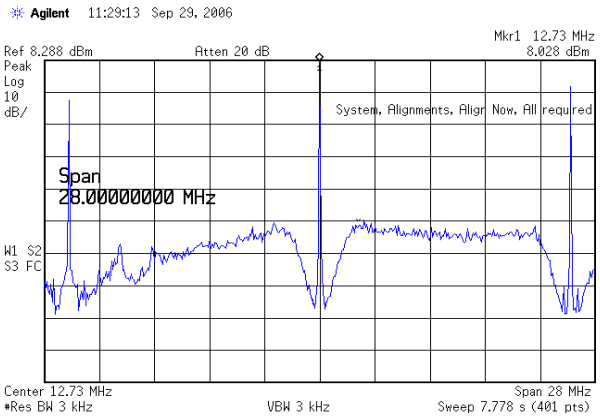

Figure 8. Measured spectrum for the 18-modulus divider at input frequency of 935 MHz and division ratio of 73.46

The loop uses a third-order type II filter with 200 kHz natural frequency, consistent with the GSM and DCS tuning time requirement, and this is reflected in the phase noise profile seen in Fig. 9.

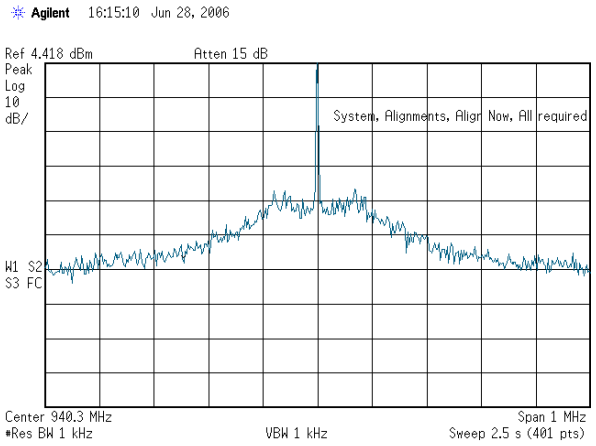

Figure 9. Frequency synthesiser output spectrum with fractional division ratio of 73.46.

IV. Conclusion

A new programmable memory controlled frequency divider has been designed and implemented. An extension of the technique has been shown that is capable of operation over a wide range of integer or fractional division ratios. The approach is particularly suited to FPGA or PLD implementation in which the entire synthesiser operation including prescaler and stored-sequence of Σ-Δ modulator can be achieved in one block. Furthermore the outputs of the fractional frequency divider are utilised as the compensating signals for the fractional-*N* synthesis. A PLL synthesiser employing these schemes has been demonstrated, confirming the agility and low phase noise expected of this approach. This synthesiser is suitable for GSM and DCS systems and a wide variety of applications.

TABLE I. Performance of the Frequency Synthesiser

fractional division ratio	73.046875 ~ 75
modulus of divider	70 ~ 77 (8 modulus)
Σ-Δ modulator	Single stage 3rd order (8-level output)
reference frquency	12.8 MHz
output frequency	935 ~ 960 MHz
Close-in phase noise	-78.92 @ 100 Hz
	-86.73 @ 1 kHz
	-94.25 @ 100 kHz

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